MOD 5 COUNTER

Specification:-

Frequency of operation-250MHz

Counting States:

000

001

010

011

100

PRE LAYOUT:-

Layout:-

Height-1.4um

Length-107um

Max frequency of operation:-

JK Flipflop- 4GHz

Counter-2GHz

DRC errors:-

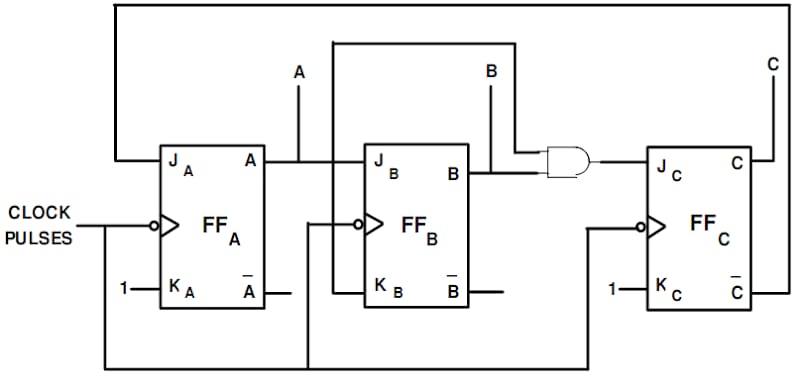
2 Density errors not addressed. All errors checked except this.

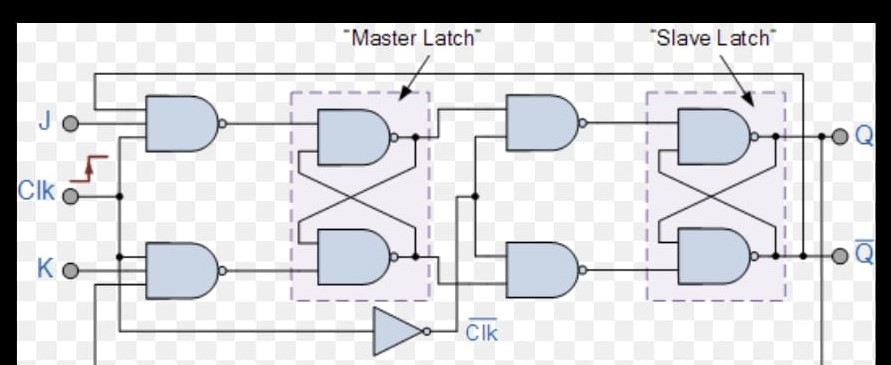
LVS errors:

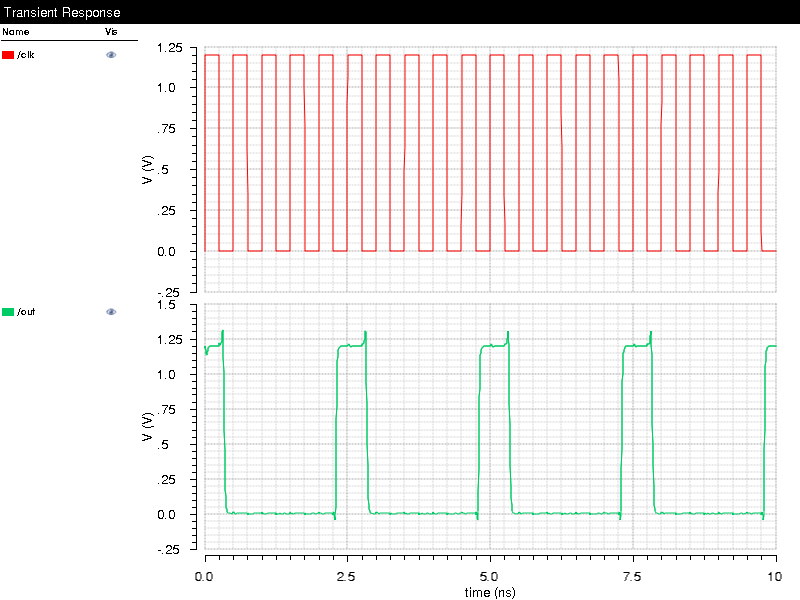
All errors checked

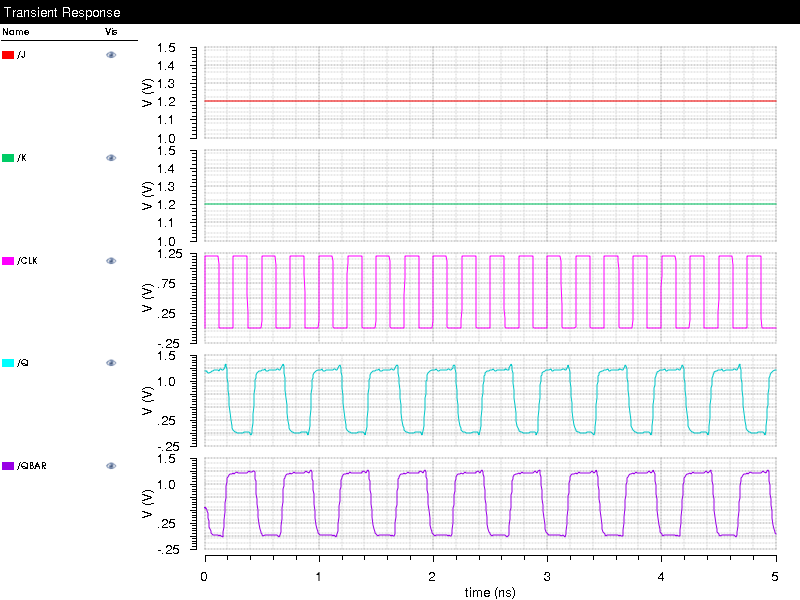
PEX errors:-

All errors checked.

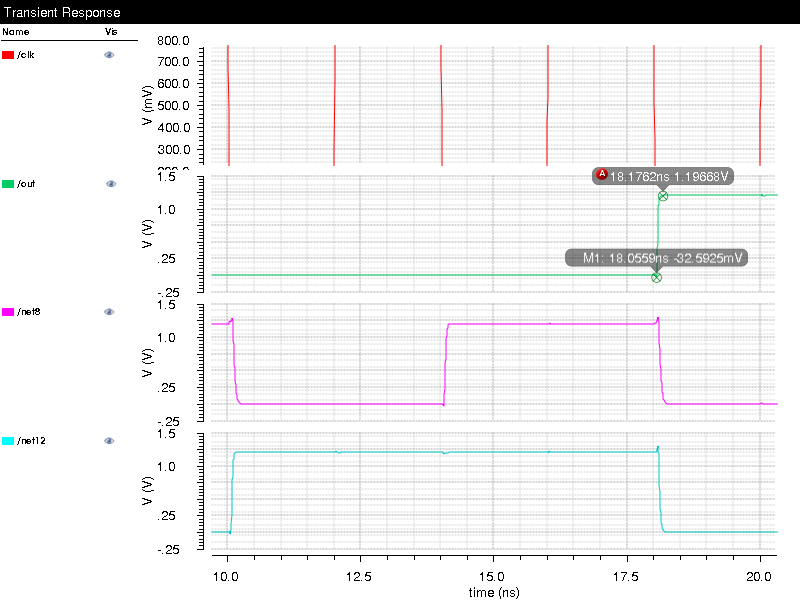


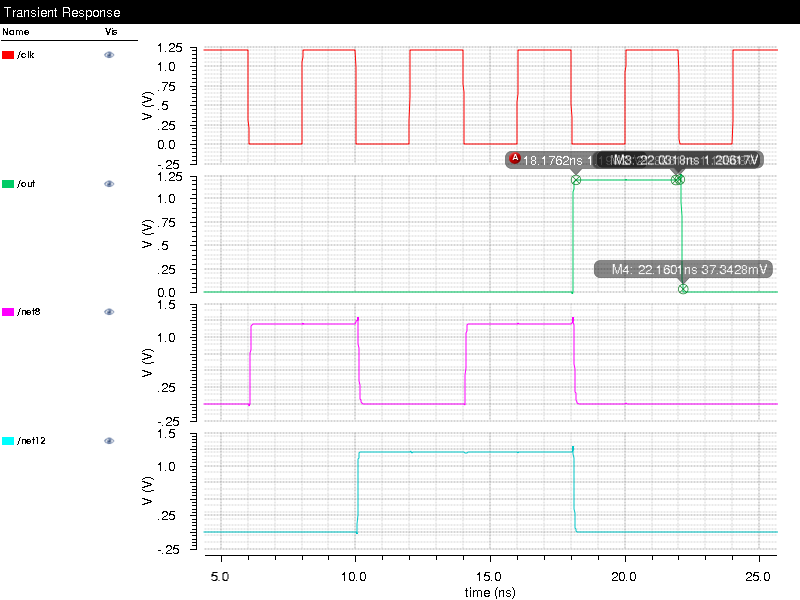


 counter at 2Ghz SCHEMATIC VIEW MAX FREQUENCY



JK FF AT 4GHz SCHEMATIC Working perfectly.

JK RISE TIME (SCHEMATIC) -.13ns

JK FLIPFLOP FALLTIME (SCHEMATIC)-.16ns

COUNTER RISE DELAY FALL TIME (PRE-LAYOUT)

For A

Rise time:50.77E-12{Expression:-riseTime(v("/A" ?result "tran") 0 nil 1.2 nil 10 90 nil "time" )}

Fall time:50.77E-12{Expression:-fallTime(v("/A" ?result "tran") 0 nil 1.2 nil 10 90 nil "time" )}

For B

Rise time:39.34E-12{Expression:-riseTime(v("/B" ?result "tran") 0 nil 1.2 nil 10 90 nil "time" )}

Fall time:39.34E-12{Expression:-fallTime(v("/B" ?result "tran") 0 nil 1.2 nil 10 90 nil "time" )}

For C

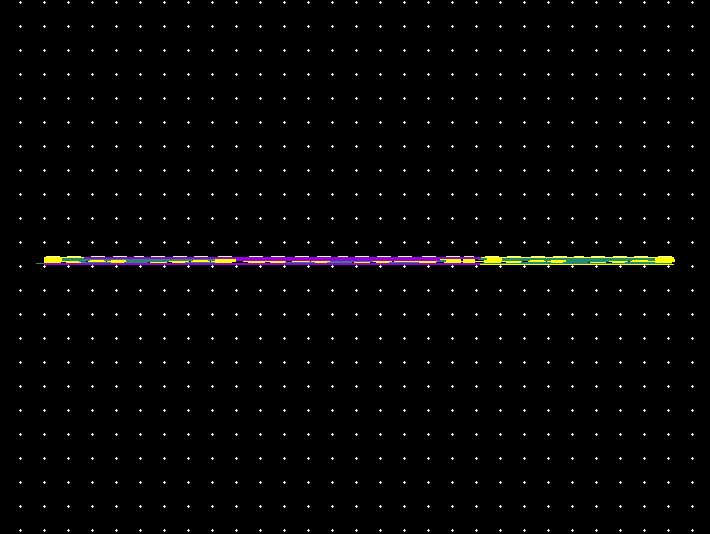
Rise time:28.67E-12{Expression:-riseTime(v("/C" ?result "tran") 0 nil 1.2 nil 10 90 nil "time" )}

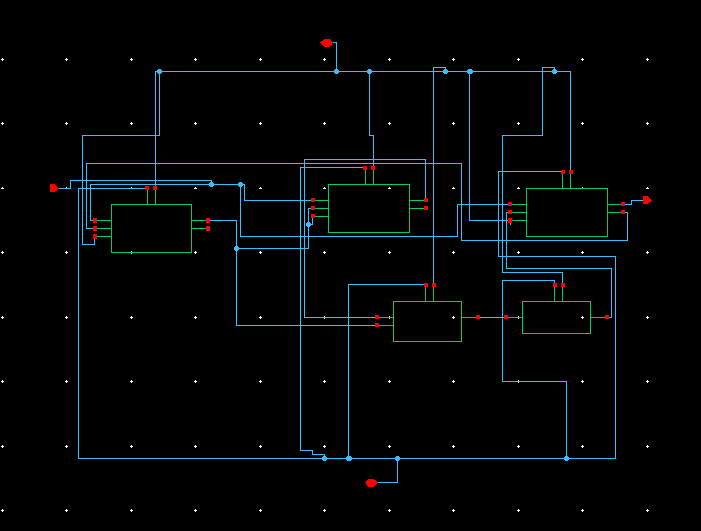
Fall time:28.67E-12{Expression:-fallTime(v("/C" ?result "tran") 0 nil 1.2 nil 10 90 nil "time" )}

Delay time (From clk to output A):32.79E-12{delay(?wf1 v("/clk\_n" ?result "tran"), ?value1 0.6, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?wf2 v("/A" ?result "tran"), ?value2 0.6, ?edge2 "rising", ?nth2 1, ?td2 nil , ?stop nil, ?multiple nil)}

Delay time (From clk to output B):65.47E-12{delay(?wf1 v("/clk\_n" ?result "tran"), ?value1 0.6, ?edge1 "falling", ?nth1 6, ?td1 0.0, ?wf2 v("/B" ?result "tran"), ?value2 0.6, ?edge2 "rising", ?nth2 1, ?td2 nil , ?stop nil, ?multiple nil)}

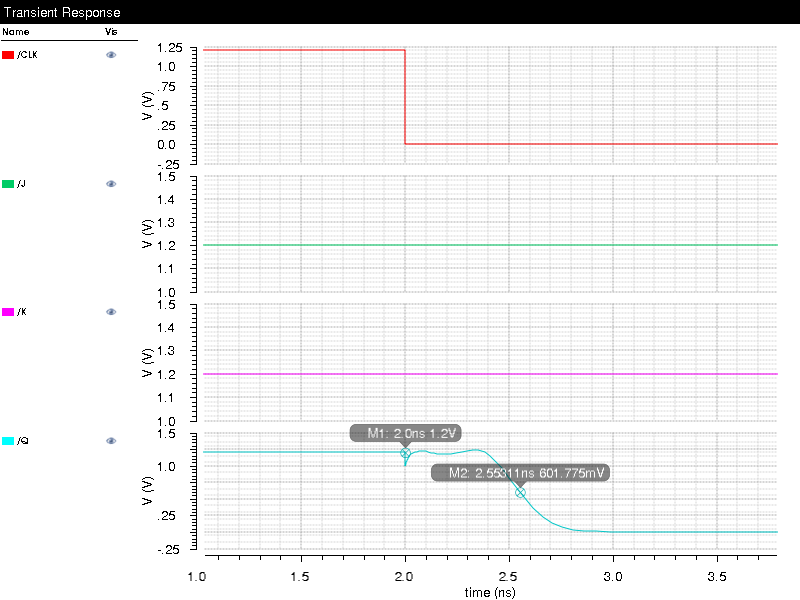
Delay time (From clk to output C):10.36E-12{delay(?wf1 v("/clk\_n" ?result "tran"), ?value1 0.6, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?wf2 v("/C" ?result "tran"), ?value2 0.6, ?edge2 "rising", ?nth2 1, ?td2 nil , ?stop nil, ?multiple nil)}

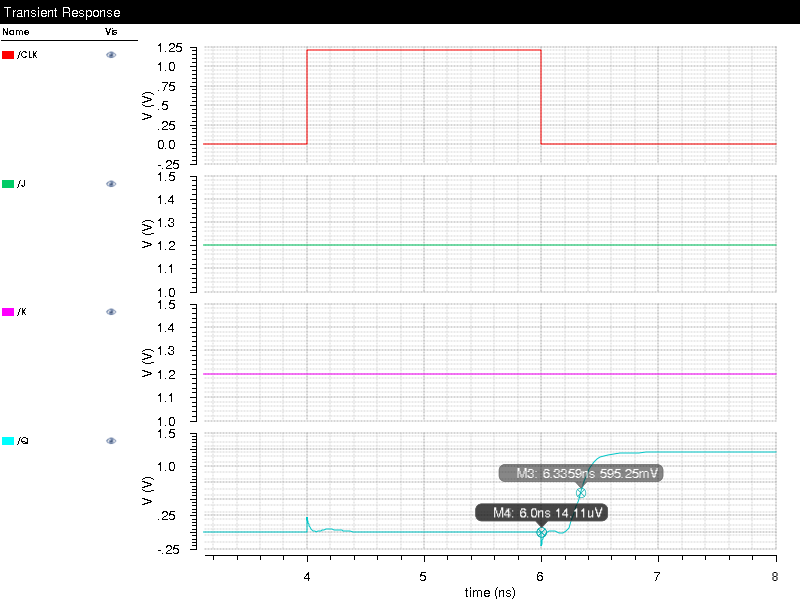
LAYOUT



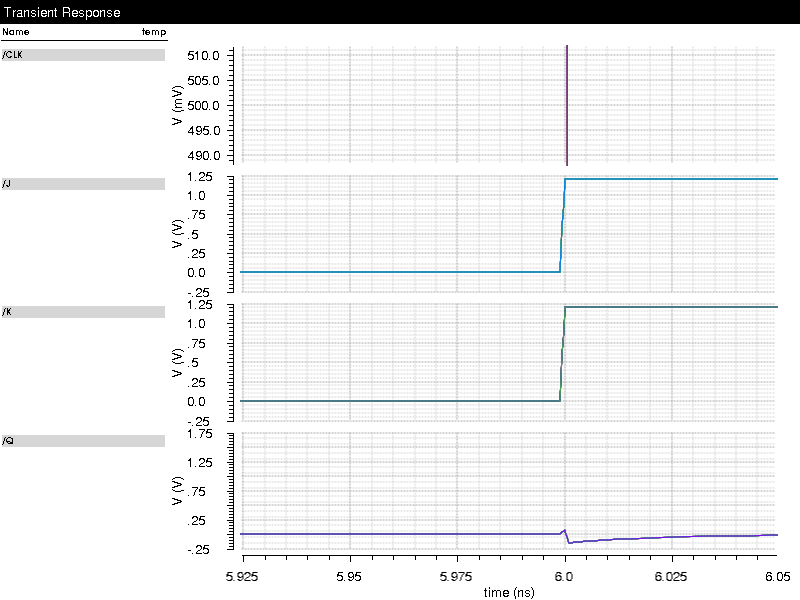
SChematic

POST-LAYOUT

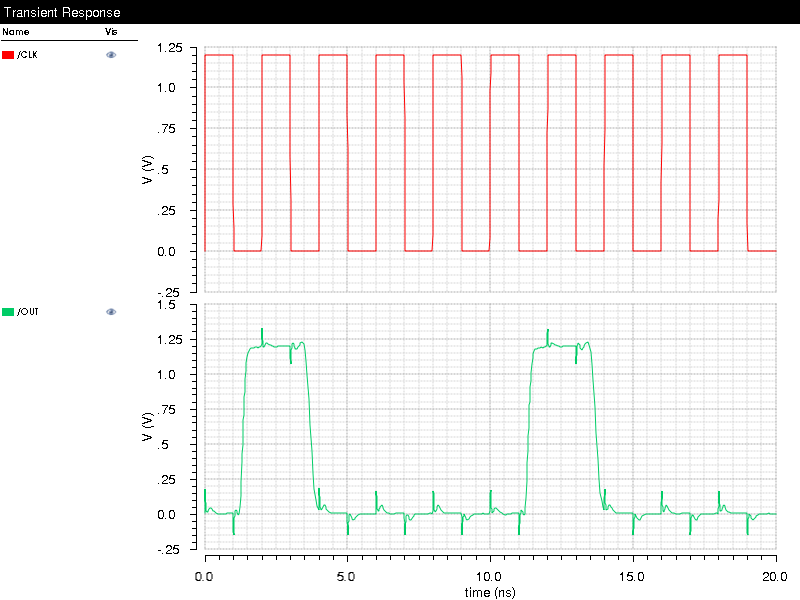
(FALL DELAY-.553ns) JK FLIP FLOP



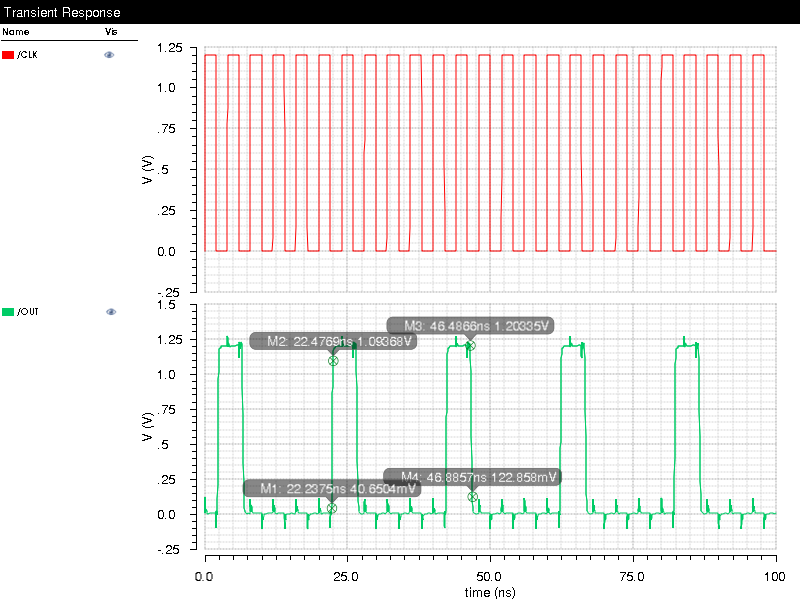
RISE DELAY TIME\_336ns JK FLIP FLOP



SETUP TIME<1ps for a spike of 1ps.



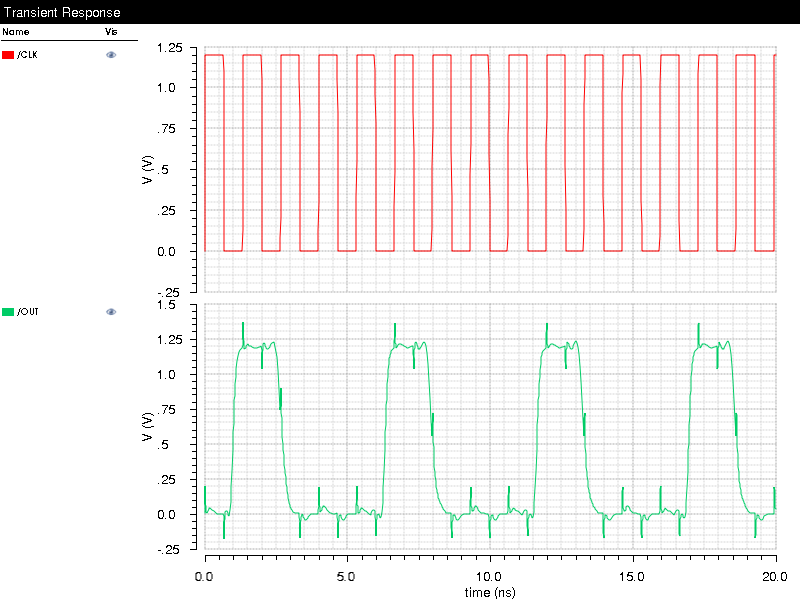
COUNTER AT 500MHz working perfect.



Rise Time of Counter -.24ns

Fall Time of Counter - .44ns

Computed at 250Mhz clock frequency.



Counter at .75GHz not working as per specification. Max Frequency- .5GHz